BooNE Technical Note 35

QT Patch Panel Design

Vern Sandberg
Los Alamos National Laboratory

Abstract

The patch panel for connecting TTL−level signals from, *e.g.*, the LSU cosmic ray counters to the dual−ported RAM registers on a modified QT card is described. The system records logic−level data in 100ns time ticks and stores it in QT RAM for later event building and collection. A single QT card has been modified to perform this task The system may be characterized as a 128−channel input register mapped onto the event data stream.

Created September 25, 2001

Introduction

A subcomponent of the calibration system for the miniBooNE experiment is the LSU cosmic ray tracking scintillator array. This is an array of scintillation counters that sit above the top hat and act as triggers for cosmic rays entering the detector. A bank of discriminators connected to the photomultiplier tubes mounted on the scintillators produce TTL−level logic pulses. In order to fold these signals into the data record for event recording the following "patch" was agreed upon:

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"muon tracker"
   TTL−level signals recorded on a modified QT Card
   to 100ns timing precision.  102 channels + 7 channels from cubes

   − LSU responsible for generation of TTL−level signals and
   cables (BNC terminated) from muon tracker electronics to QT
   electronics.  Routing to be determined, but must not compromise
   detector signals.

   − Los Alamos responsible for BNC patch panel to connect into a
   modified QT card.  Modification will consist of connecting
   inputs to the 16 dual−port memories, resulting in a total of 16
   x 8 = 128 digital channels recorded every 100ns.  Signal levels
   are "slow" TTL.
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(From an email summarizing the interface between the LSU supplied detectors and the LANL supplied DAQ electronics, reproduced in this document as Appendix A.)

Recording the timing of these pulses to 100ns resolution was deemed to be adequate for reconstruction of the cosmic rays' trajectories with sufficient accuracy for calibration purposes. Therefore, it was decided that modifying a QT card to introduce the counter data into the data stream at the dual−ported memory would meet the data recording needs. The counter data would then be registered in 100ns increments and aligned with the co−recorded detector data. It would be collected using the existing QT crate system with the acquisition code modified to read the bit pattern of "on counters". This code element resides in the monoboard computer residing in the individual QT crate. (This code needs to be written.)

The hardware to provide this capability consists of two 5U x 19" aluminum panels configured with 64 BNC jacks on each panel. The interface circuitry is located on printed circuit cards that have 8 BNC jacks on one edge and a 16−pin header on the other edge. Eight of these cards fill out one panel. The 16−pin header connects to an IDC twisted−pair plug and cable, which in turn connects to 8 channels of modified QT dual−port RAM. There are 16 of these cable assemblies, each cable connecting to an 8−bit RAM on the modified QT card. All of this is illustrated in Fig. 1.

The detector signals are connected to the QT card RAM through an on−card bus between the FADCs and the dual−port RAMs. In normal operation this bus is driven by the FADCs, but for the recording of counter signals we disable the FADCs by putting their outputs in the high impedance state (this is a 3−state bus) by disabling the ENABLE pins on the FADCs and connecting a twisted pair cable between the digital ground and the relevant input lines to the RAMs. A 16−pin in−line header soldered to the back side of the QT card at the input pins on the RAMs provides a convenient connection point and accepts the cable from the patch panel pc cards. (This modification is reversible, so the QT card is not damaged.)

Motivation and Electrodynamics

The "electronics" (or rather the electrodynamics) that makes this whole thing interesting is how to match the signals from their TTL source to the load presented by the RAM. A model of the input and output circuits of a "typical" CMOS device is shown in Fig. 2.

We will assume that the electronics producing the logic signals looks something like the cascaded CMOS transistors shown in this figure. For our purposes we consider the circuit to be a voltage source with a small (something like 10 ohms) series resistance connected to a length of 50 ohm coaxial cable. This cable connects to the BNC patch panel. At the other end is a CMOS input, modeled by two large resistors (relatively speaking) and a 15 pF capacitor to ground. This is connected to a twisted−pair cable that leads to the patch panel IDC connector. Twisted pair cable has an impedance of approximately 100 ohms and is "balanced". This means that there is democracy between the two wires, unlike the coaxial cable that has an inner conductor and an outer braid. This configuration is shown in Fig. 3.

We want clean signals at the input to our memory. They should look like square TTL−level pulses (0 V for a logical "low" and something greater than 2 V for a logical "high"). We also do not want to burn out the driver electronics, so we must keep its DC load as large as is possible. Cables have the habit of bouncing pulses back and forth at their terminals due to impedance mismatches and we want to make our system as immune as is possible to this and still be consistent with the other constraints outlined above. To be captured by the 100 ns clock the pulses must be greater than 100ns wide. In practice they should be greater than 200ns to have a safe margin of being high when the clock tick occurs.

The circuitry on the pc card in the patch system provides the compromise solution to these requirements. It back terminates the 100 ohm twisted−pair cables through the two 25 ohm resistors and the 50 ohm coaxial cable. This keeps the signal at the memory clean. The connection at the memory is "open" in order to gain a doubling of the terminal voltage and ease the requirements on the driver electronics at the other end. A pulse does travel back down the coaxial cable and may be reflected depending on the nature of the driver (whether it is terminated in 50 ohms or not), but event if it is reflected it will be attenuated an arrive at the memory at a voltage less than the logic threshold level and not be recorded. This sequence is demonstrated in the SPICE simulation described in the next section.

Circuit Description and Simulation

The discriminator signals are assumed to come from TTL−level cable drivers that produce 0 to > 2 V pulses, but not necessarily back terminated in 50 ohms. This last point greatly reduces the requirements on the cable drivers (it is easier to drive 100 ohms or 50 ohms than it is to drive 25 ohms). The design of the patch circuit mitigates the influence of the driver termination on the signal that appears at the memory−end of the cable. This is the reason for this tech note. A simple patch panel would have serious problems connecting a 50 ohm coaxial cable signal to a 100 ohm twisted−pair cable that was terminated in 1k ohm shunted by 15 pF of capacity. (These values approximate what the memory input looks like electrically.)

The signals from the discriminators are connected through 50 ohm coaxial cables to the BNC jacks on the printed circuit cards. The BNC jacks are isolated from one another and from "ground". On a printed circuit card the coaxial cable leads (shield and center conductor) are connected to the leads of 100 ohm twisted−pair cable through two 25 ohm resistors, a resistor in series on each lead. This arrangement preserves the balance of currents flowing in the shield and center conductor of the coaxial cable. The configuration provides a 100 ohm back termination for the twisted−pair cable. The other end of the twisted−pair cable is connected to the input−ground pair of connections of the QT dual−ported RAM. The circuit described is shown in Fig. 3 and the SPICE netlist is shown below.

The memory electronics requires the signal voltage to exceed 1.5 V to be detected as a logical high ("H") signal. (We said greater than 2 V above, the 1.5 V is closer to the TTL threshold, but the 2 V specification gives a better noise margin.) TTL−line drivers typically send 2 V pulses into 50 ohm loads and are not back terminated. (We are taking a "worst case" situation.) The history of a pulse train as it travels through the system is shown from a SPICE simulation in Figs. 5, 6 and in a real system in Fig. 7. The study of a pulse train (instead of just a single pulse) is relevant because of the importance in

determining the effects of the build up of reflections in the transmission lines and the resultant distortion. As can be seen by close inspection of the figures, the patch system delivers pulses of appropriate pulse height and width to be sensed as valid high logic pulses. The effect of reflections is a dropping of the base line to negative voltages, but the resultant is small enough to have no effect on the CMOS memory.

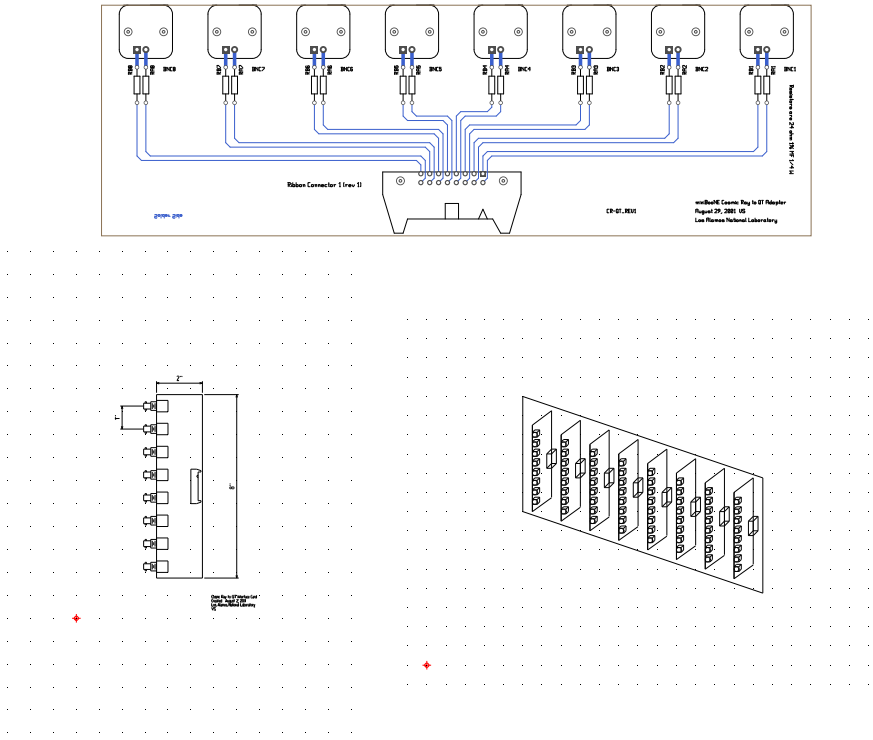

Fig. 1 Panel and card configuration and layout. Twisted−pair ribbon cable connects onto IDC−style headers on the backs of the circuit cards.

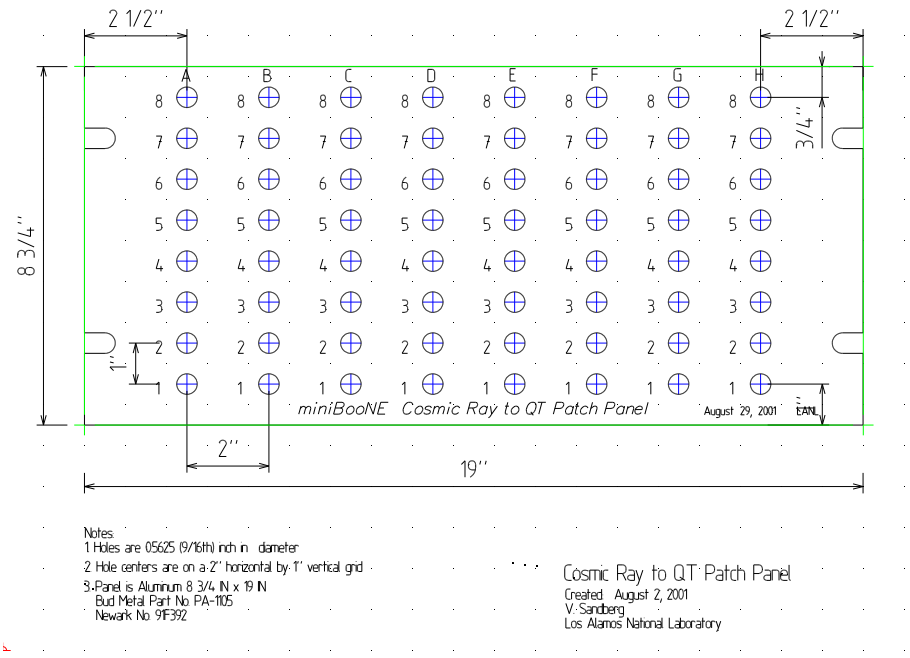

Fig. 2 Front panel design. BNC jacks are on a 2" x 1." grid, 8 rows by 8 columns.

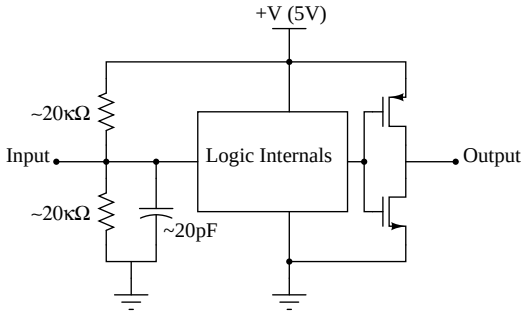

Fig. 3 Schematic model of the input and output circuitry of a CMOS device.

Simulation netlist:

```
cr−qt.cir
R19 2 1 10
R20 N002 7 1K
V13 1 0  pulse 0 2 0 10ns 10ns 100ns 300ns
V14 N001 0  0
V15 N003 0  0
T7 2 N001 3 4 Td=200n Z0=50
T8 5 6 7 N004 Td=200n Z0=100
R22 6 N003 100MEG
R23 5 3 25
R24 6 4 25
V16 N004 0  0
C4 7 N004 15pF
.tran 2ns 5000ns 0 .1ns
.end
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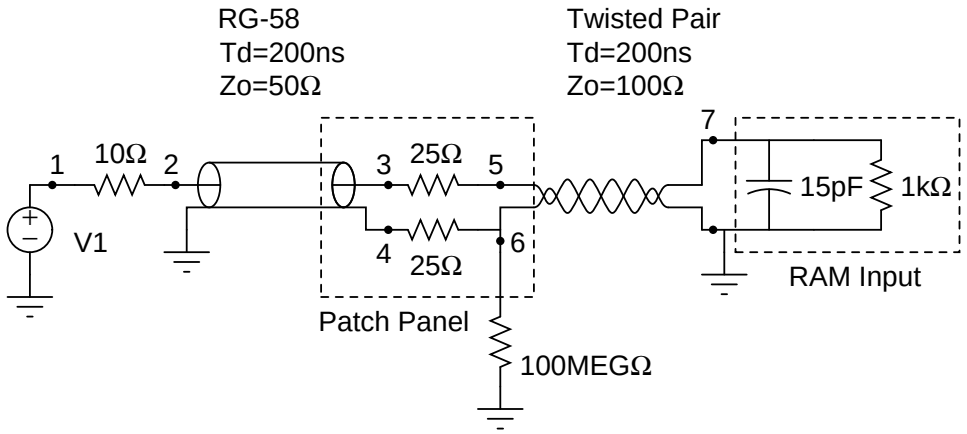

Fig. 4 Circuit modeling the pulse transmission lines between the TTL−source and the CMOS memory destination.

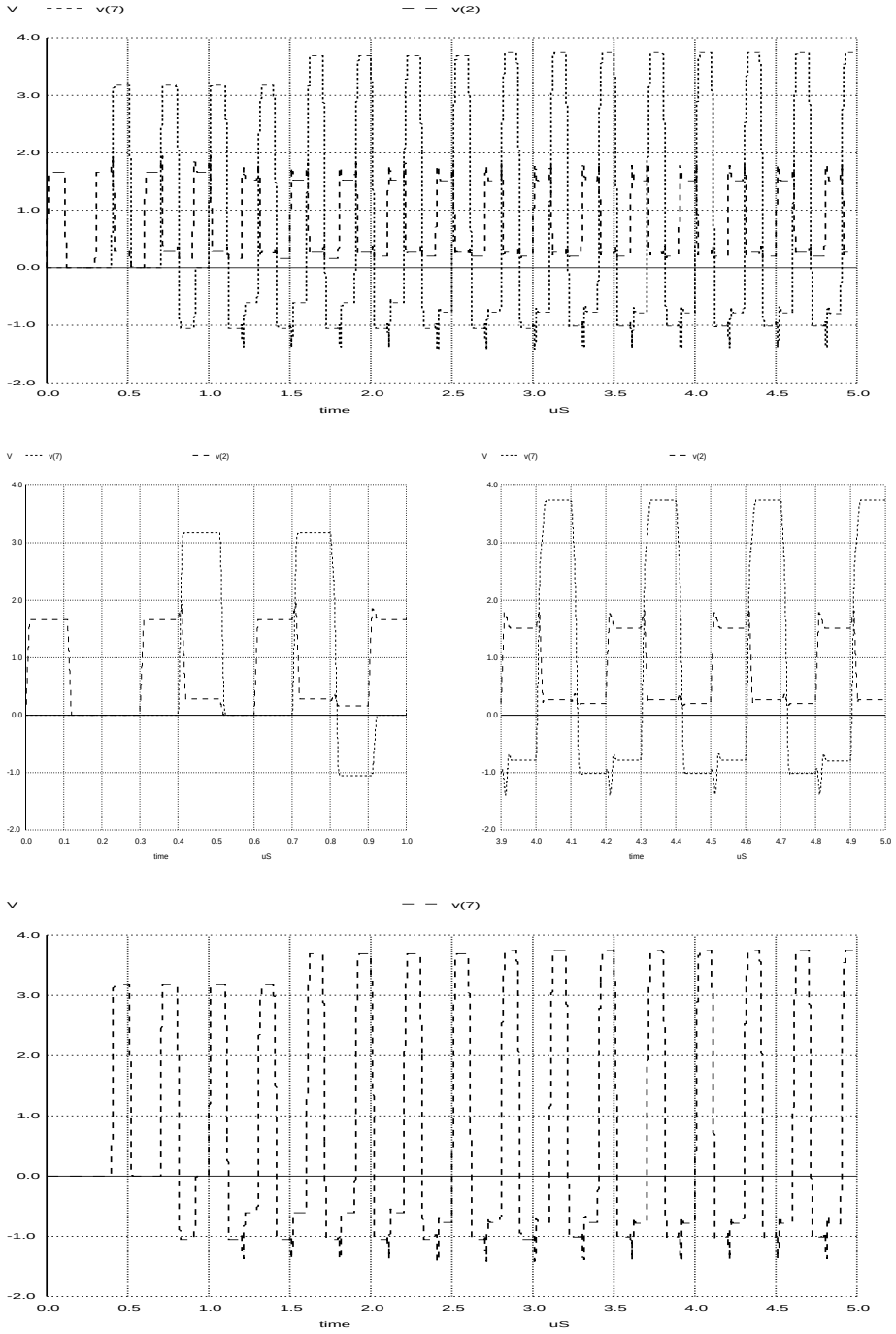

Fig. 5 SPICE simulation waveforms of voltage nodes as shown on Fig. 4. The nodes shown here are at the driving point and at the termination at the CMOS memory, modeled as a resistive load shunted by a 15 pF capacitor.

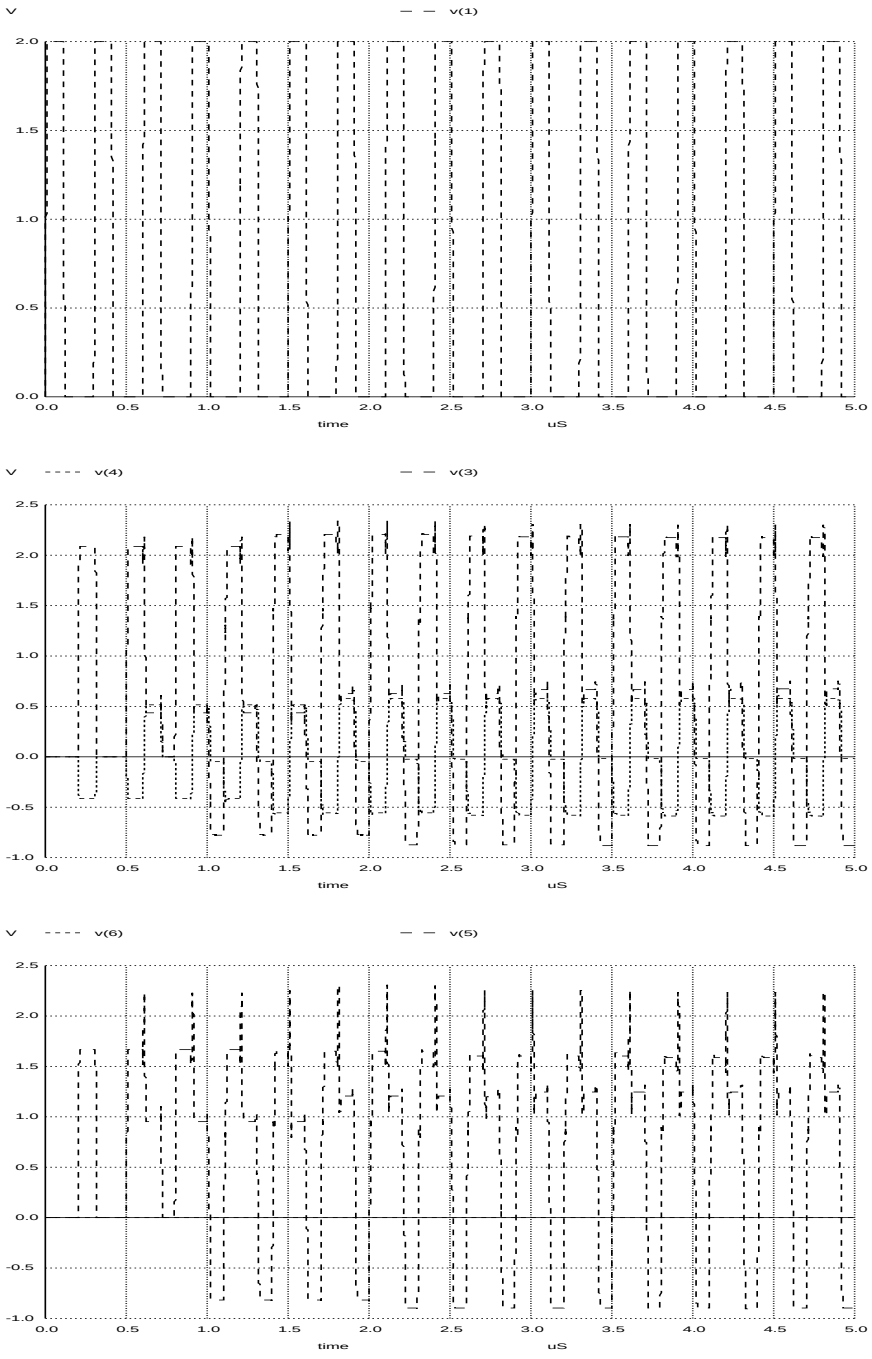

Fig. 6 Continuation of SPICE simulation waveforms of voltage nodes as shown on Fig. 4. The nodes shown here are at the midpoint where the coaxial cable joins onto the twisted−pair cable.

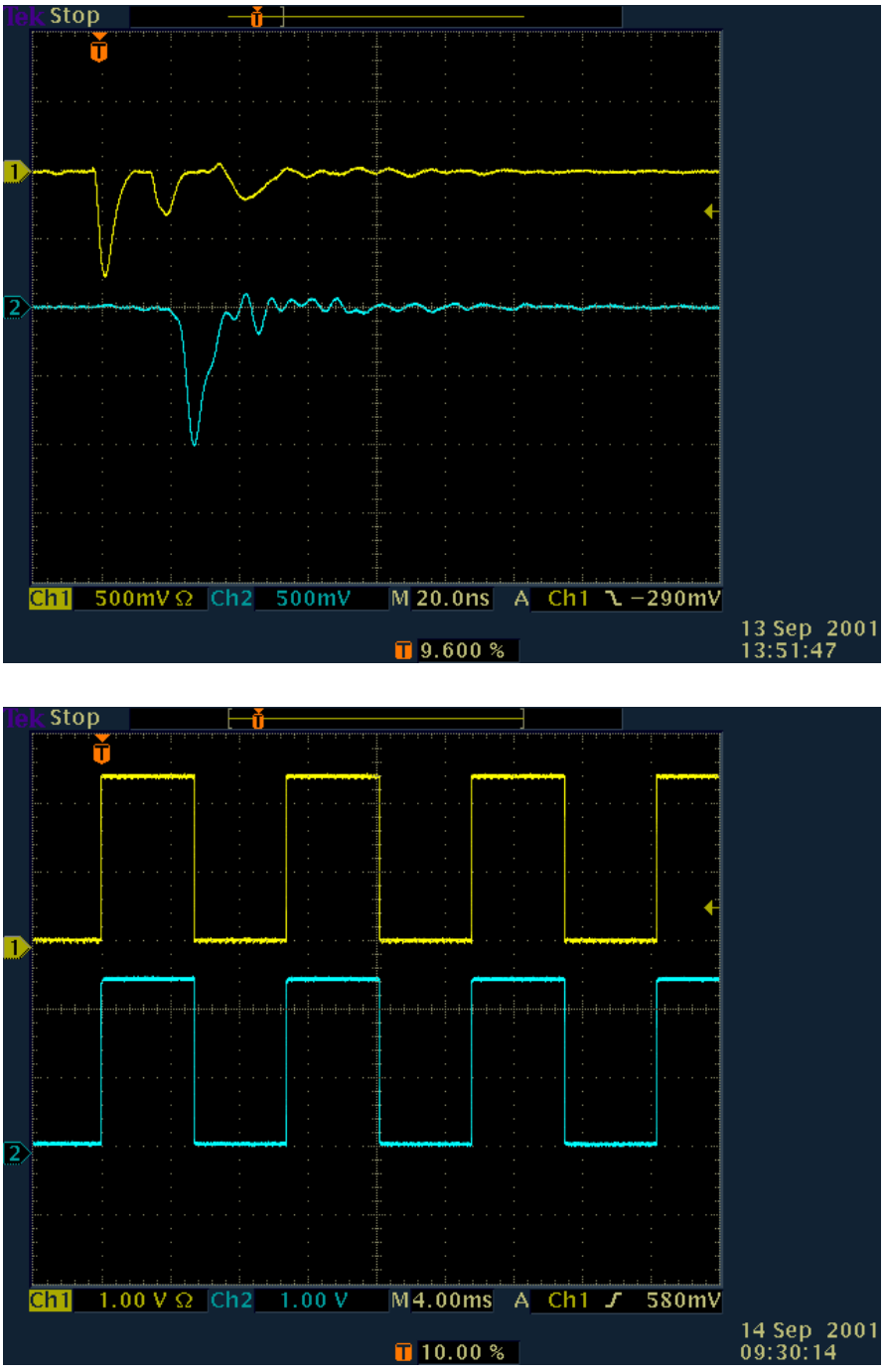

Fig. 7 Voltage waveform at the terminal end of the patch system. The top picture shows the transfer for a fast pulse. The bottom picture shows the approach to equilibrium of a pulse train.

Appendix A

Letter Defining the Calibration Interface to DAQ

Date: Wed, 31 Jan 2001 11:47:34 −0700 (MST)
From: Vern Sandberg <sandberg@p25hp.lanl.gov>
To: layabouts@nu1.lampf.lanl.gov
Subject: calibration interface to DAQ

MiniBooNE Calibration System: Signal Interface to MiniBooNE DAQ

Notes from a telephone conference between Los Alamos and LSU on the interfacing of the calibration system signals into the data acquisition and trigger systems.

Date of tele−conference: Wednesday, January 31, 2001

Attendees: V. Sandberg, R. Schirato (Los Alamos)
M. Sung, R. Imlay (LSU)

1. "cubes"
   scintillation signals from 3/4" pmts
   7 channels of low level pmt signals, dynamic range −20mV to −2V.
   − LSU responsible for anode signal pickoffs and patch panel with BNC connections.
   − Los Alamos responsible for BNC−qt input cables to connect from patch panel to QT cards.
   (use 8th channel for recording laser timing pulse)

2. "muon tracker"
   TTL−level signals recorded on a modified QT Card to 100ns timing precision. 102 channels + 7 channels from cubes

   − LSU responsible for generation of TTL−level signals and cables (BNC terminated) from muon tracker electronics to QT electronics. Routing to be determined, but must not compromise detector signals.

   − Los Alamos responsible for BNC patch panel to connect into a modified QT card. Modification will consist of connecting inputs to the 16 dual−port memories, resulting in a total of 16 x 8 = 128 digital channels recorded every 100ns. Signal levels are "slow" TTL.

3. "trigger"
   A variety of signals need to be provided to the trigger system to flag and/or enable triggering to record the relevant calibration data. The calibration trigger types are:
   a) cube signal
   b) tracker signal
   c) laser trigger
   Note: a) and b) will be "anded" with a detector multiplicity signal.

   LSU expressed a wish for a "2.2MeV" trigger in a 1msec window, similar to the LSND trigger system. The DAQ team needs to evaluate the feasibility of adding this trigger. The concern is a compromise of the run stream timing (increased latency) and in coordinating and synchronizing the data streams. More on this later. [VS]

   Signals into the trigger system should be either NIM or TTL. The old LSND system used NIM−level signals. The MiniBooNE system is still under design and the signal types may change. This will be resolved soon. [VS]